



## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

Sheet 1

of 2

Application Number	10/826,463
Filing Date	April 16, 2004
First Named Inventor	David G. Nairn
Art Unit	2819
Examiner Name	Leah Nguyen
Attorney Docket Number	A3GN2504US

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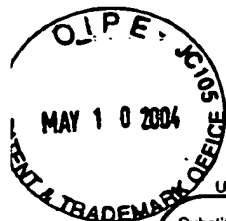
**Examiner  
Signature**

Date Considered

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

**Complete if Known**

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Art Unit	2819
Examiner Name	Linh Nguyen
Attorney Docket Number	A3GN2504US

Sheet	2	of	2
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**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
L	1	CONROY et al, Parallel Pipeline A/D Converter in 1-um CMOS, IEEE Journal of Solid-State Circuits, Vol.28. No. 4, April 1, 1999, P.447-454.	
L	2	FU et al, Digital Background Calibration Technique, IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998, P.1904 - 1991.	
L	3	DYER et al, Analog Background Calibration Technique, IEEE Journal of Solid-State Circuits, Vol. 33, No. 12, December 1998, P.1912-1919.	
L	4	SUMANEN et al, CMOS Parallel Pipeline A/D Converter, IEEE Journal of Solid-State Circuits, Vol. 36, No. 7, July 2001, P1048-1055.	
L	5	HUMMELS et al, Distortion Compensation for Time-Interleaved Analog to Digital Converters, IEEE 1996, P.728-731.	
		Linh Van Nguyen	

Examiner Signature	<i>Linh Van Nguyen</i>	Date Considered	1/03/05
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